PALCE22V10Q-25

us$ 7.20

24-Pin E^2 CMOS Programmable Array Logic (PAL®)

DISTINCTIVE CHARACTERISTICS

- Electrically Erasable (E^2) device using AMD's advanced CMOS EEPROM technology
- Reprogrammable cells allow AC and DC testing to be performed at the factory
- PRELOAD feature for improved testability
- Product-term-driven synchronous-PRESET and asynchronous-RESET
- 25-ns Quarter-Power (55 mA) commercial temperature range devices
- 33-MHz external frequency
- Output logic macrocell and varied product-term distribution for enhanced flexibility
  - Registered or combinatorial outputs
  - Programmable output polarity
- Supported by PALASM2 software

GENERAL DESCRIPTION

The PALCE22V10Q is the most popular second-generation Programmable Array Logic (PAL) device. It utilizes the familiar sum-of-products (AND-OR) logic structure with an AMD-invented Output Logic Macrocell (macrocell). This enables the PALCE22V10Q to replace LSI functions of 700-to-800-equivalent gate complexity, with the inherent advantages of programmable logic.

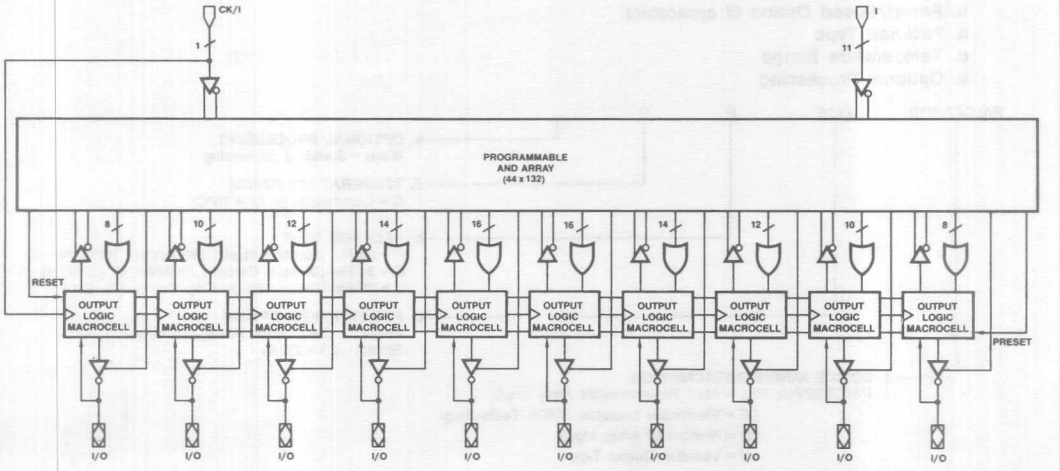
The PALCE22V10Q features variable product-term distribution, where 8 to 16 logical product terms are allocated to each output (see Block Diagram for distribution details). This feature allows for more complex functions to be implemented than were possible in previous devices.

System operation has been enhanced by the addition of synchronous-PRESET and asynchronous-RESET product terms. These terms are common to all output flip-flops.

The PALCE22V10Q also incorporates power-up RESET, and the capability to PRELOAD the output registers to any desired state during testing. PRELOAD enhances the device testability and permits easy logic verification.

The Macrocell allows the designer the flexibility to individually configure the architecture of each output according to the application requirements. Each macrocell is programmable to allow the Input/Output pin to be configured as an input or an output, on a dynamic or permanent basis, by means of an output-enable product term. With 12 dedicated inputs and 10 configurable macrocells this allows up to 22 inputs and 10 outputs. Each output is user-programmable for registered or combinatorial operation, and can also be fed back into the array.

BLOCK DIAGRAM



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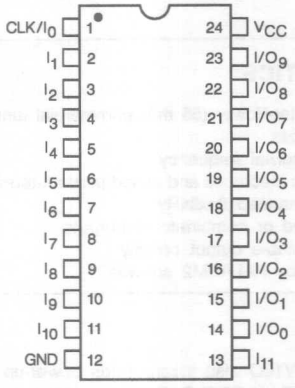
CONNECTION DIAGRAMS
Top View

SKINNY DIP



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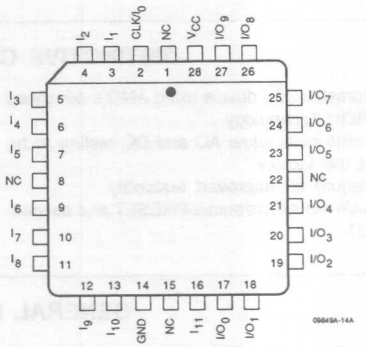

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Pin Designations:

I	= Input
I/O	= Input/Output
V_{CC}	= Supply Voltage
GND	= Ground
CLK	= Clock
NC	= No Connection

Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Programmable Array Logic (PAL) Products

AMD PAL products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Power/Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

PALCE22V10 Q-25 P C _

e. OPTIONAL PROCESSING
Blank = Standard processing

d. TEMPERATURE RANGE
C = Commercial (0 to +75°C)

c. PACKAGE TYPE
P = 24-Pin (300-Mil) Plastic SKINNYDIP (PD3024)
D = 24-Pin (300-Mil) Ceramic SKINNYDIP (CD3024)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)

b. POWER/SPEED OPTION
Power: Q = Quarter Power (55 mA)
Speed: -25 = 25 ns

a. DEVICE NUMBER/DESCRIPTION
PALCE22V10: PAL = AMD Programmable Array Logic
CE = Electrically Erasable CMOS Technology
22 = Number of Array Inputs
V = Versatile Output Type
10 = Number of Flip-Flops

Valid Combinations	
PALCE22V10Q-25	PC, DC, JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

FUNCTIONAL DESCRIPTION

The PALCE22V10Q contains an Electrically Erasable programmable cell array organized in the familiar sum-of-products (AND-OR) structure.

The Block Diagram details the basic architecture. Up to 22 inputs and 10 outputs are available. Each input is connected to a programmable-AND array containing 120 logical product terms. Initially the AND gates are disconnected from both the TRUE and COMPLEMENT of every input. By selectively programming the E^2 cells, the AND gates may be "connected" to only the TRUE input, to only the COMPLEMENT input, or to both types of input. When both the TRUE and COMPLEMENT inputs are connected, a logical-FALSE results on the output of the AND gate. The outputs of the AND gates are connected to fixed-OR gates with an average of 12 product terms. The number of product terms per OR gate has been distributed from 8 to 16 to allow more complex logical functions to be performed with a single PAL device.

Output Logic Macrocells

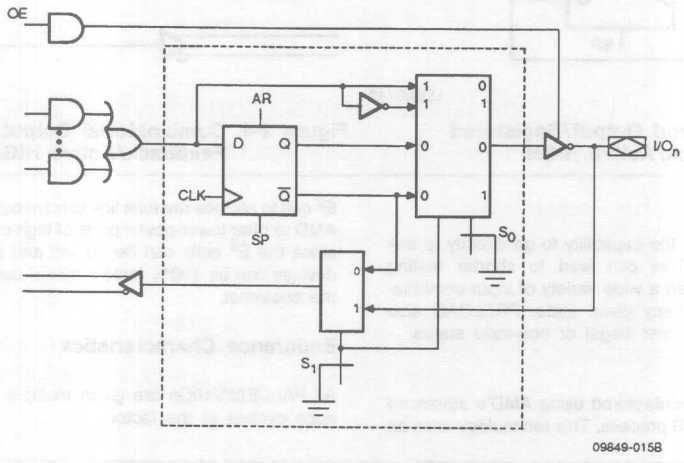
A dramatic innovation in programmable-logic architecture is the AMD-invented Macrocell. This allows the user to program the function of the outputs on an output-by-output basis.

PALCE22V10Q

As shown in Figure 1, the PALCE22V10Q Macrocell contains two programmable E^2 cells (S_0 and S_1). S_0 controls the output polarity (active HIGH or active LOW). S_1 controls whether the output and feedback path will be combinatorial or registered (note that these functions are not independent). Depending on the states of these two cells, an individual output will operate in one of four modes (Figure 2): 1) Registered Output/Registered Feedback/Active LOW; 2) Registered Output/Registered Feedback/Active HIGH; 3) Combinatorial Output/Combinatorial Feedback/Active LOW; or 4) Combinatorial Output/Combinatorial Feedback/Active HIGH. This macrocell gives the designer flexibility, and enables the device to be optimized for the precise application. It also allows better device utilization — allowing programming for only as many registers as needed.

PRESET/RESET

To improve in-system functionality, the PALCE22V10Q has additional PRESET and RESET product terms. These terms are connected to all registered outputs. When the synchronous-PRESET product term is asserted (HIGH), the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the asynchronous-RESET product term is asserted (HIGH), the output registers will be immediately loaded with a LOW, independent of the clock. These functions are particularly useful for applications such as system power-on and reset.



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OE = Output-Enable Product Term
AR = Common Asynchronous-RESET Product Term
SP = Common Synchronous-PRESET Product Term

Figure 1. PALCE22V10Q Output Logic Macrocell Diagram

S_1	S_0	Output Configuration
0	0	Registered/Active LOW
0	1	Registered/Active HIGH
1	0	Combinatorial/Active LOW
1	1	Combinatorial/Active HIGH

0 = Programmed State (discharged or connected)
1 = Erased State (charged or disconnected)

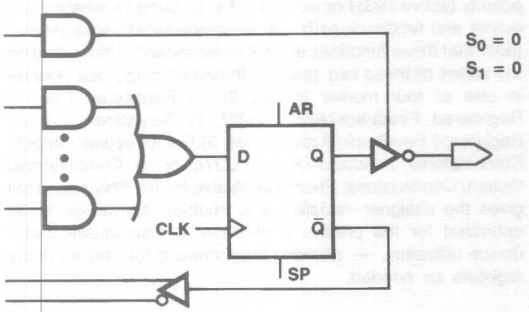


Figure 2-1. Registered Output/Registered Feedback/Active LOW

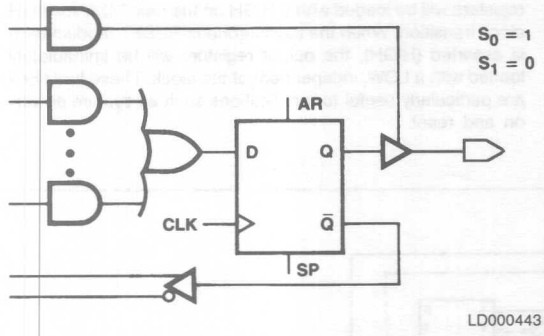


Figure 2-2. Registered Output/Registered Feedback/Active HIGH

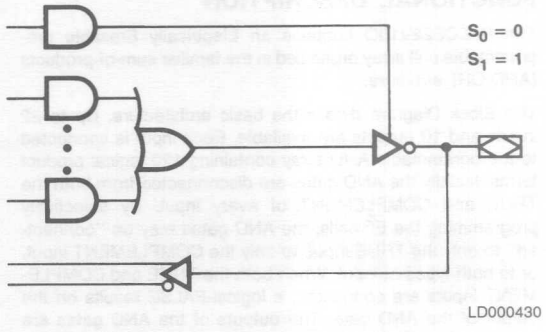


Figure 2-3. Combinatorial Output/Combinatorial Feedback/Active LOW

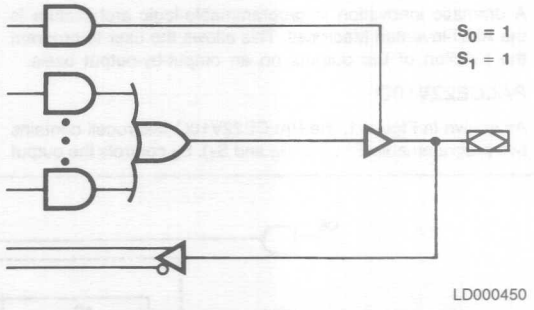


Figure 2-4. Combinatorial Output/Combinatorial Feedback/Active HIGH

PRELOAD

PRELOAD mode provides the capability to go directly to any desired arbitrary state. This can lead to shorter testing sequences, especially when a wide variety of input combinations must be tested for any given state. PRELOAD also provides the capability to test illegal or non-valid states.

Fabrication

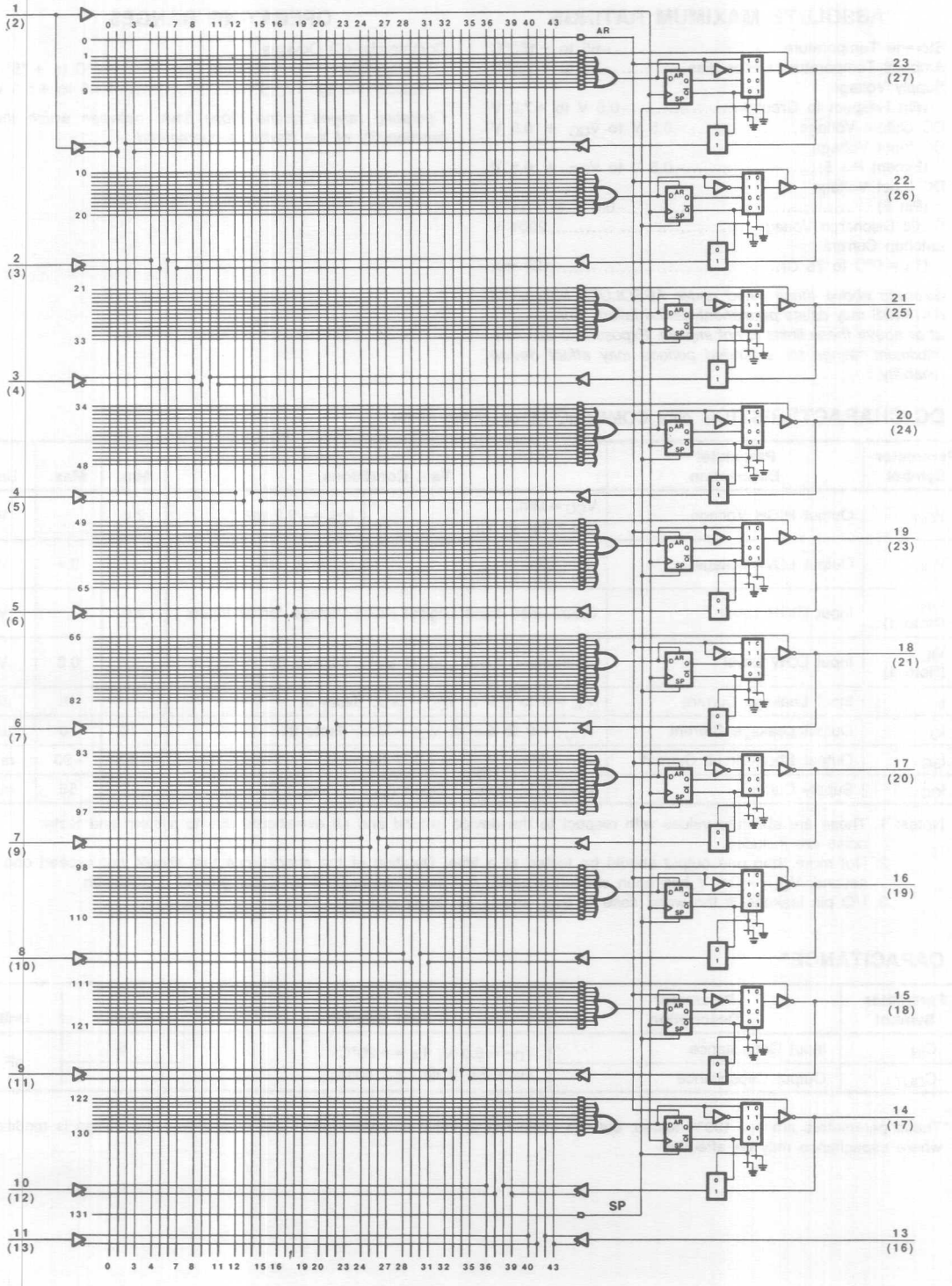
The PALCE22V10Q is manufactured using AMD's advanced Electrically Erasable CMOS process. This technology uses an E^2 cell to replace the fuse link used in bipolar parts, and allows AMD to offer lower-power parts of high complexity. In addition, since the E^2 cells can be erased and reprogrammed, these devices can be 100% factory tested before being shipped to the customer.

Endurance Characteristics

All PALCE22V10Qs are given multiple erase cycles (endurance cycles) at the factory.

Endurance Characteristics

Symbol	Parameter	Value	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
N	Min. Reprogramming Cycles	100	Cycles	Operating Conditions



DIP (PLCC) Pinouts

Figure 3. PALCE22V10Q Logic Diagram

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature Under Bias ..... −55 to +125°C
Supply Voltage
with Respect to Ground ..... −0.5 V to +7.0 V
DC Output Voltage ..... −0.5 V to V_{CC} + 0.5 V
DC Input Voltage
(Except Pin 5) ..... −0.5 V to V_{CC} + 0.5 V
DC Input Voltage
(Pin 5) ..... −0.6 V to +11 V
Static Discharge Voltage ..... 2001 V
Latchup Current
(T_A = 0°C to 75°C) ..... 100 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A) Operating Free Air ..... 0°C to +75°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating range

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA		0.4	V
V_{IH} (Note 1)	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for all Inputs		2.0		V
V_{IL} (Note 1)	Input LOW Level	Guaranteed Input Logical LOW Voltage for all Inputs			0.8	V
I_I	Input Leakage Current	V_{IN} = 0 to 5.5 V, V_{CC} = Max. (Note 3)			10	μA
I_O	Output Leakage Current	V_{OUT} = 0 to 5.5 V, V_{CC} = Max. (Note 3)		−10	10	μA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.5 V (Note 2)		−30	−90	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_O = 0), V_{CC} = Max.			55	mA

Notes: 1. These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.
2. Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.
3. I/O pin leakage is the worst case of I_{OZL} and I_{IL} (or I_{OZH} and I_{IH}).

CAPACITANCE*

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{CC} = 5.0 V, T_A = +25°C V_{IN} = 2.0 V @ f = 1 MHz	5	pF
C_{OUT}	Output Capacitance		8	

*These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

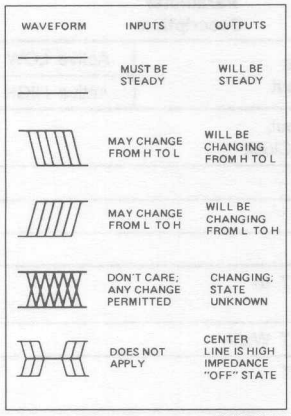
SWITCHING CHARACTERISTICS over COMMERCIAL operating range (Note 1)

Parameter Symbol	Parameter Description			PALCE22V10Q-25 Min.	PALCE22V10Q-25 Max.	Unit
t_{PD}	Input or Feedback to Non-Registered Output		Active LOW		25	ns
			Active HIGH			
t_S	Setup Time from Input, Feedback or SP to Clock			15		ns
t_H	Hold Time			0		ns
t_{CO}	Clock to Output				15	ns
t_{CF}	Clock to Feedback				13	ns
t_{AR}	Asynchronous RESET to Registered Output				25	ns
t_{ARW}	Asynchronous RESET Width			25		ns
t_{ARR}	Asynchronous RESET Recovery Time			25		ns
t_{SPR}	Synchronous PRESET Recovery Time			25		ns
t_{WL}	Width of Clock		LOW	13		ns
t_{WH}			HIGH	13		ns
f_{MAX}	Maximum Frequency (Note 2)	Internal Feedback $1/(t_S + t_{CF})$		35.7		MHz
		External Feedback $1/(t_S + t_{CO})$		33.3		
t_{EA}	Input to Output Enable				25	ns
t_{ER}	Input to Output Disable				25	ns

Notes: 1. Commercial Test Conditions: $R_1 = 300\ \Omega$, $R_2 = 390\ \Omega$ (see switching test circuit.)
2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS



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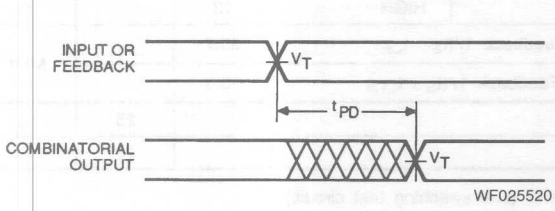

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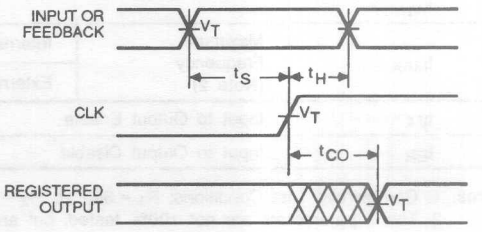
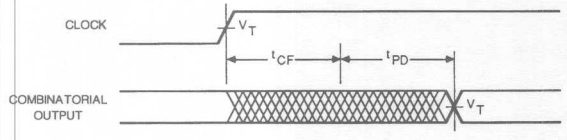
Combinatorial Output



WF025571

Registered Output



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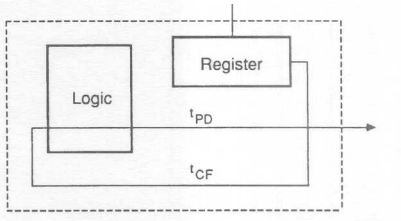
Clock to Feedback to Combinatorial Output (See Path at Right)



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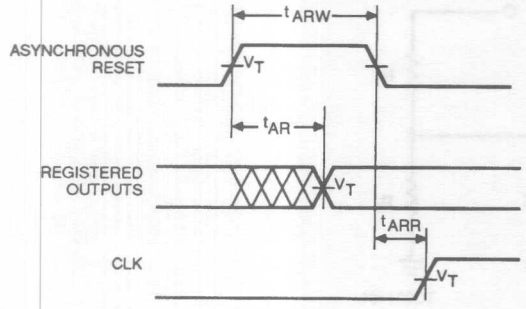
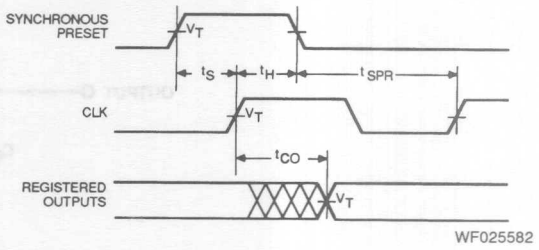
SWITCHING WAVEFORMS (Cont'd.)



WF025602

Asynchronous RESET



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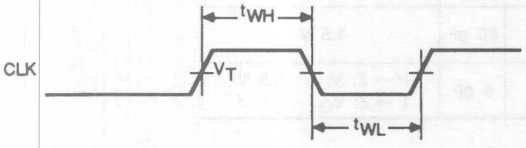
Synchronous PRESET



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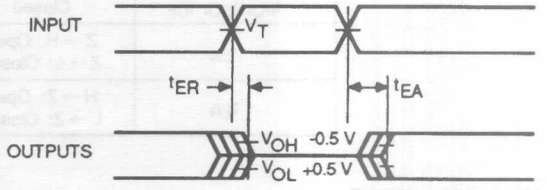
Clock Width

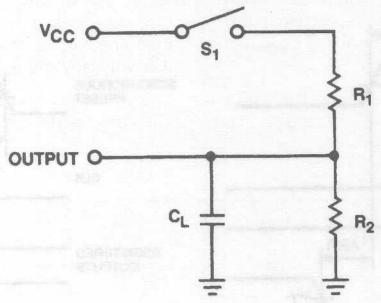


WF025612

Input-to-Output Disable/Enable

Notes: 1. $V_T = 1.5$ V
2. Input pulse amplitude 0 to 3.0 V.
3. Input rise and fall times 2-5 ns typical.

SWITCHING TEST CIRCUIT



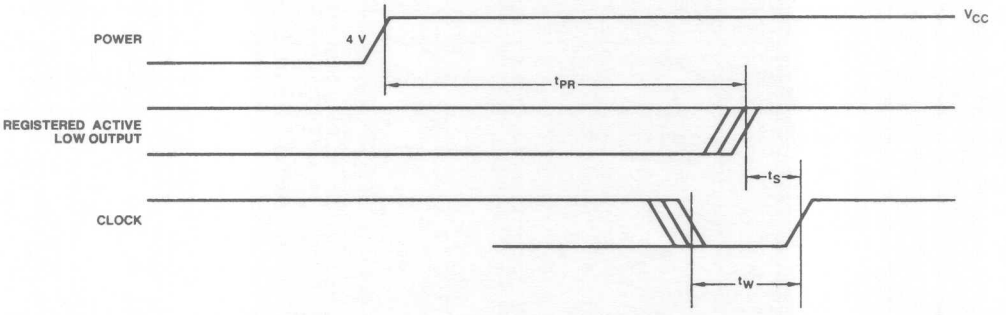
TC001191

TEST OUTPUT LOADS (R_1 = 300 Ω, R_2 = 390 Ω)			
Specification	**Switch S_1**	**C_L**	**Measured Output Value**
t_{PD}, t_{CO}, t_{CF}	Closed	50 pF	1.5 V
t_{EA}	Z → H: Open Z → L: Closed	50 pF	1.5 V
t_{ER}	H → Z: Open L → Z: Closed	5 pF	H → Z: V_{OH} −0.5 V L → Z: V_{OL} +0.5 V

Power-Up RESET

The registered devices in the PALCE22V10Q have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to LOW. The output state will depend on the polarity of the output buffer. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the asynchronous operation of the power-up reset, and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.



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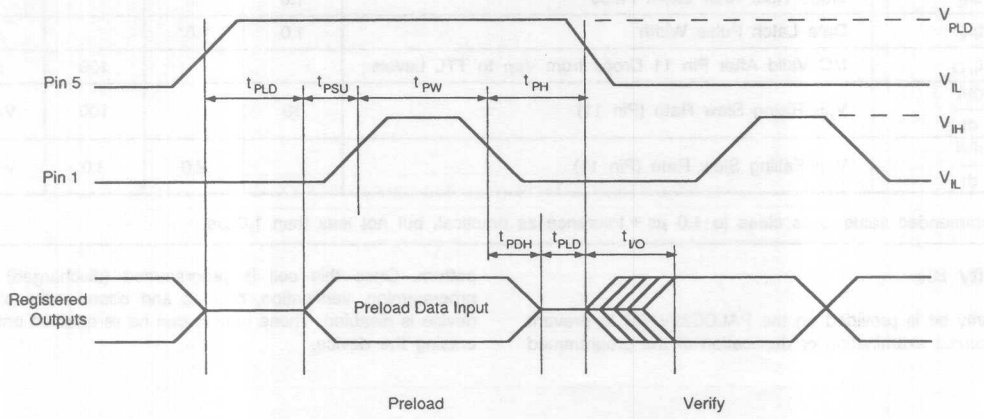
Parameter Symbol	Parameter Description	Min.	Max.	Unit
t_{PR}	Power-Up Reset Time		10	μs
t_S	Input or Feedback Setup Time	See Switching Characteristics		
t_W	Clock Width			

Preload of Registered Outputs

The PALCE22V10Q registered outputs are provided with circuitry to allow loading each register synchronously with either a HIGH or LOW. This feature simplifies testing since any state can be loaded into the registers to control test sequencing.

A typical function test sequence would be to verify all possible state transitions for the device being tested. This requires the ability to force the state registers into an arbitrary "present state" value. Once this is done, the state machine is then clocked into a new state, or "next state". The next state is then checked to validate transition from the present state. In this way any state transition can be checked.

The pin levels and timing necessary to perform the Preload function are detailed below.



WF026810

TABLE 1. PRELOAD AC ELECTRICAL CHARACTERISTICS (T_A = 25°C ±5°C)

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{PLD}	PRELOAD Voltage	9.5	10	10.5	V
V_{ILP}	Input LOW Level During Preload/Verify	0	0	0.5	V
V_{IHP}	Input HIGH Level During Preload/Verify	3.0	4.0	V_{CC}	V
V_{OL}	Verify LOW		0.3	0.5	V
V_{OH}	Verify HIGH	2.4	3.4		V

Note: AC undershoot on any input should be limited to −1 V.

TABLE 2. PRELOAD AC ELECTRICAL CHARACTERISTICS (T_A = 25°C ±5°C)

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
t_{PLd}	Setup and Hold Data to Preload (Pin 5)	50	50		μs
t_{PSU}	Data Setup Prior to Applying PRELOAD Latch Pulse	1.0	1.0*		μs
t_{Pdh}	Data Hold After Latch Pulse	1.0	1.0*		μs
t_{Ph}	Mode Hold After Latch Pulse	1.0	1.0*		μs
t_{Pw}	Data Latch Pulse Width	1.0	1.0*		μs
$t_{I/O}$	I/O Valid After Pin 11 Drops from V_{PP} to TTL Levels			100	μs
$\frac{dVr}{dt}$	V_{PP} Rising Slew Rate (Pin 11)	10		100	V/μs
$\frac{dVf}{dt}$	V_{PP} Falling Slew Rate (Pin 11)		2.0	3.0	V/μs

*Recommended value is as close to 1.0 μs + tolerance as practical, but not less than 1.0 μs.

Security Bit

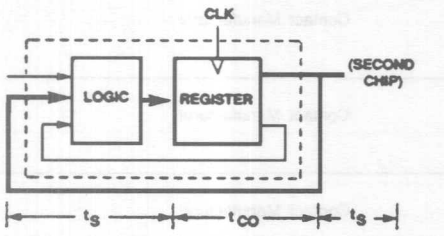
A security bit is provided on the PALCE22V10Q to prevent unauthorized examination or duplication of the programmed pattern. Once this cell is programmed (discharged), the programming, verification, preload and observability of the device is disabled. These modes can be re-enabled only by erasing the device.

f_{MAX} PARAMETERS

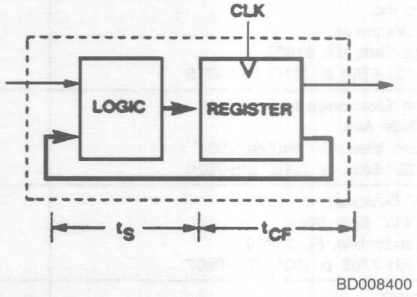
The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified for two types of synchronous designs.

The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX} external."

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs ($t_S + t_{CF}$). This f_{MAX} is designated "f_{MAX} internal."



f_{MAX} External Feedback; $1/(t_S + t_{CO})$



f_{MAX} Internal Feedback; $1/(t_S + t_{CF})$

Programmers/Development Systems (Subject to change)

MANUFACTURER	PROGRAMMER CONFIGURATION
Adams MacDonald 800 Airport Road Monterey, CA 93940 (408) 373-3607	Contact Manufacturer
Data I/O Corporation 10525 Willows Road NE PO Box 97046 Redmond, WA 98073-9746 (800) 247-5700	UniSite 40 REV 2.6
Digelec Inc. 22736 Vanowen Canoga Park, CA 91307 (800) 367-8750 or (818) 887-3755	Contact Manufacturer
Kontron Electronics Inc. 630 Clyde Ave. Mountain View, CA 94039-7230 (800) 227-8834 or (415) 965-7020	Contact Manufacturer
Logical Devices 1201 N.W. 65th Place Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967	Contact Manufacturer
Microprоss Parc d'Activite des Pres 5, rue Denis-Papin 59650 Villeneuve-d'Ascq (20) 47.90.40	Contact Manufacturer
Stag Microsystems 1600 Wyatt Dr., Suite 3 Santa Clara, CA 95054 (408) 988-1118	Contact Manufacturer
Varix Corporation 1210 E. Campbell Rd. Suite 100 Richardson, TX 75081 (214) 437-0777	Contact Manufacturer

MANUFACTURER	SOFTWARE DEVELOPMENT SYSTEM
Advanced Micro Devices, Inc. 901 Thompson Place Sunnyvale, CA 94088-3453 (800) 222-9323	PALASM® 2 Software, rev. 2.22 and later
Data I/O Corporation 10525 Willows Road NE PO Box 97046 Redmond, WA 98073-9746 (800) 247-5700	ABEL™ Software, rev. 2.0 and later
Logical Devices 1201 E. Northwest 65th Pl. Fort Lauderdale, FL 33309 (800) 331-7766 or (305) 974-0967	CUPL™ Software, rev. 2.11 and later

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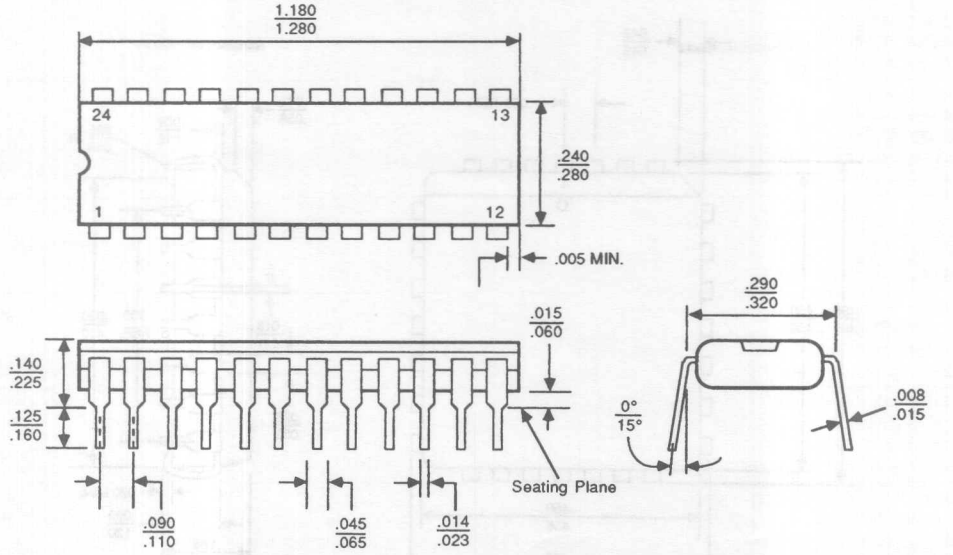
PHYSICAL DIMENSIONS*

PD3024



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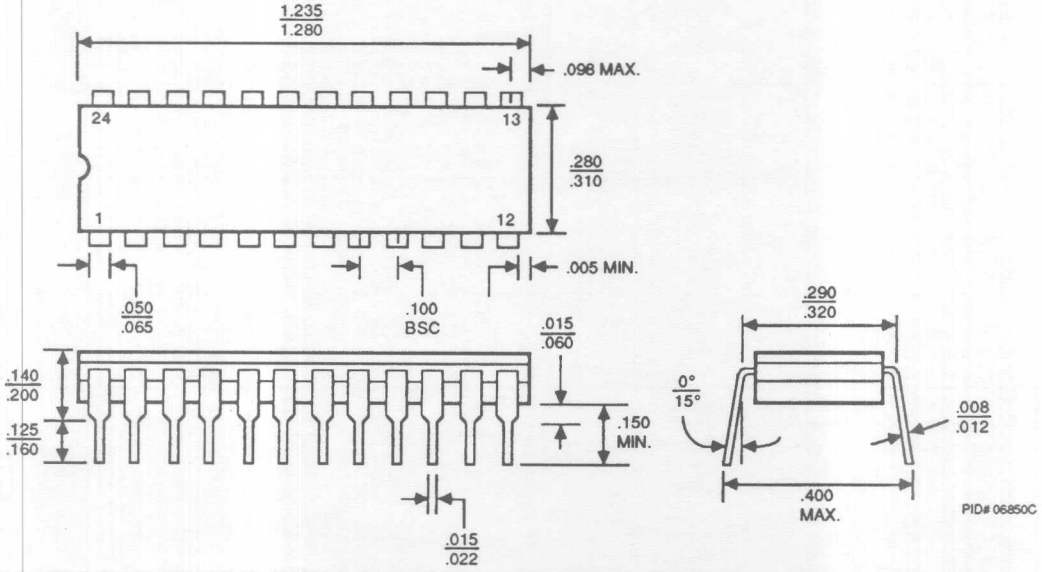

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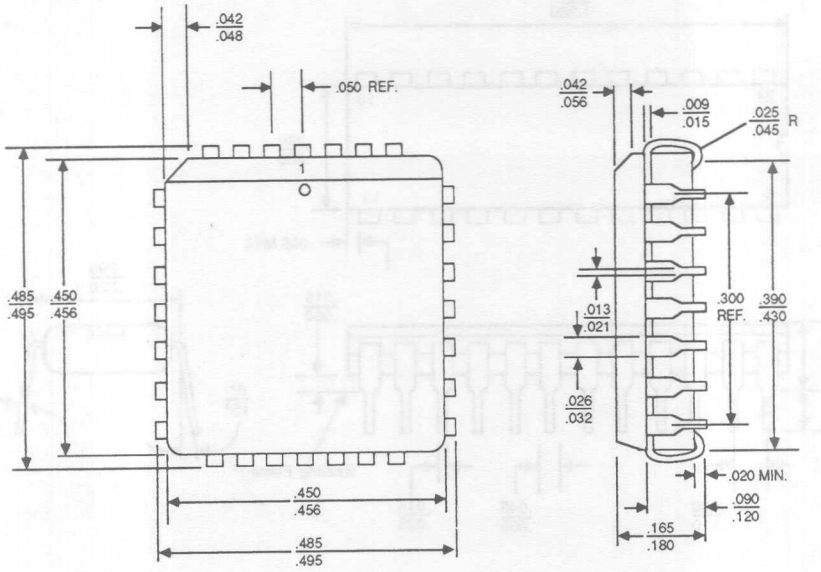
*For reference only. All dimensions are measured in inches. BSC is an ANSI standard for Basic Space Centering.

PHYSICAL DIMENSIONS (Cont'd.)

PL 028



PID # 06751E

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Advanced Micro Devices, Inc. 901 Thompson Place, P.O. Box 3453, Sunnyvale, CA 94088, USA
Tel: (408) 732-2400 • TWX: 910-339-9280 • TELEX: 34-6306 • TOLL FREE: (800) 538-8450
APPLICATIONS HOTLINE TOLL FREE: (800) 222-9323 • (408) 749-5703

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